Topological index calculation of DAEs in circuit simulation

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Abstract. Electric circuits are present in a number of applications, e.g. in home computers, television, credit cards, electric power networks, etc. The development of integrated circuit requires numerical simulation. Modern modeling techniques like the Modified Nodal Analysis (MNA) lead to differential algebraic equations (DAEs). Properties like the stability of solutions of such systems depend strongly on the DAE index.
The paper deals with lumped circuits containing voltage sources, current sources as well as general nonlinear but time-invariant capacitances, inductances and resistances. We present network-topological criteria for the index of the DAEs obtained by the classical and the charge oriented MNA. Furthermore, the index is shown to be limited to 2 for our model-class.

Key words. Circuit simulation, integrated circuit, differential-algebraic equation, DAE, index, modified nodal analysis, MNA

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1 Basics of electric circuit analysis

Consider lumped electric circuits containing resistances, capacitances, inductances, voltage sources and current sources. For two-terminal (one-port) lumped elements, the current through the element and the voltage across it are well-defined quantities. For lumped elements with more than two terminals, the current entering any terminal and the voltage across any pair of terminals are well defined at all times (cf. [2]). Hence, general time-invariant n-terminal resistances can be modeled by an equation system of the form

$$i_k = g_k(v_1, ..., v_{n-1}) \quad \text{for} \quad k = 1, ..., n-1$$

if i_k represents the current entering terminal k and v_l describes the voltage across the pair of terminals $\{l, n\}$ (for $k, l = 1, ..., n-1$). In this case, we call the terminal n the reference terminal. For electrotechnical reasons, the current entering terminal n is given by $i_n = -\sum_{k=1}^{n-1} i_k$. The conductance matrix $G(v_1, ..., v_{n-1})$ is defined by the Jacobian

$$G(v_1, ..., v_{n-1}) := \begin{pmatrix} \frac{\partial g_1}{\partial v_1} & \cdots & \frac{\partial g_1}{\partial v_{n-1}} \\ \vdots & \ddots & \vdots \\ \frac{\partial g_{n-1}}{\partial v_1} & \cdots & \frac{\partial g_{n-1}}{\partial v_{n-1}} \end{pmatrix}.$$

Correspondingly, the capacitance matrix $C(v_1, ..., v_{n-1})$ of a general nonlinear n-terminal capacitance is given by

$$C(v_1, ..., v_{n-1}) := \begin{pmatrix} \frac{\partial q_1}{\partial v_1} & \cdots & \frac{\partial q_1}{\partial v_{n-1}} \\ \vdots & \ddots & \vdots \\ \frac{\partial q_{n-1}}{\partial v_1} & \cdots & \frac{\partial q_{n-1}}{\partial v_{n-1}} \end{pmatrix}$$

if the voltage-current relation is defined by means of charges by

$$i_k = \frac{d}{dt} q_k(v_1, ..., v_{n-1}) \quad \text{for} \quad k = 1, ..., n-1.$$

Inductances can be modeled by means of fluxes by

$$v_k = \frac{d}{dt} \phi_k(i_1, ..., i_{n-1}) \quad \text{for} \quad k = 1, ..., n-1.$$

Then, the inductance matrix $L(i_1, ..., i_{n-1})$ is given by the Jacobian

$$L(i_1, ..., i_{n-1}) := \begin{pmatrix} \frac{\partial \phi_1}{\partial i_1} & \cdots & \frac{\partial \phi_1}{\partial i_{n-1}} \\ \vdots & \ddots & \vdots \\ \frac{\partial \phi_{n-1}}{\partial i_1} & \cdots & \frac{\partial \phi_{n-1}}{\partial i_{n-1}} \end{pmatrix}.$$

Assume all voltage and current sources to be *independent* sources for a while. At the end of the paper we will generalize the main results for some controlled sources.

One of the most commonly used network analyses in circuit simulation is the Modified Node Analysis (MNA). It represents a systematic treatment of general circuits and is important when computers perform the analysis of networks automatically. The MNA uses as the vector of unknowns all node voltages and branche currents of current controlled elements. Performing the MNA means:

1. Write node equations by applying KCL (Kirchhoff's Current Law) to each node except for the datum node:

$$Aj = 0. \tag{1}$$

The vector j represents the branch current vector. The matrix A is called the (reduced) incidence matrix and describes the network graph, the branche-node relations. Moreover, it holds

$$a_{ik} = \begin{cases} 1 & \text{if branch } k \text{ leaves node } i \\ -1 & \text{if branch } k \text{ enters node } i \\ 0 & \text{if branch } k \text{ is not incident with node } i \end{cases}$$

for the elements of A.

2. Replace the currents j_k of voltage controlled elements by the voltage-current relation of these elements in equation (1).

3. Add the current-voltage relations for all current controlled elements.

Note, in case of multi-terminal elements with n terminals we speak of branches if they represent a pair of terminals $\{l, n\}$ with $1 \leq l \leq n$.

Split the incidence matrix A into the element-related incidence matrices $A = (A_C A_L A_R A_V A_I)$, where A_C, A_L, A_R, A_V and A_I describe the branch-current relation for capacitive branches, inductive branches, resistant branches, branches of voltage sources and branches of current sources, respectively. Denote by j_L and j_V the current vector of inductances and voltage sources. Defining by i_s and v_s the vector of functions for current and voltage sources, respectively, we obtain the following equation system by applying the MNA:

$$\begin{aligned} A_C \frac{dq(A_C^T e)}{dt} + A_R g(A_R^T e) + A_L j_L + A_V j_V + A_I j_s &= 0, & (2) \\ \frac{d\phi(j_L)}{dt} - A_L^T e &= 0, & (3) \\ A_V^T e - v_s &= 0. & (4) \end{aligned}$$

2 DAE index of the network equations

The solution behaviour of DAEs depends stronlgy on the index of DAEs. Generally, numerical difficulties increase with higher index (see e.g. [1], [5], [7]). Very roughly speaking, if a network equation system contains algebraic equations, but the solution does not depend on the derivatives of input functions, then we speak of index-1 systems. If the solution depends on the first derivative of input functions, but it does not depend on higher order derivatives, then we speak of index-2 systems. An accurate and practical description of index is given by the tractability concept (see [7]), which we use in this paper.

Let us write the network equations (2)-(4) in MNA formulation as a quasilinear DAE

$$A(x)\dot{x} + b(x) = r. \tag{5}$$

The vector x contains the node potentials e (excepting the datum node), the branch currents j_L of inductances and the branch currents j_V of the voltage sources. Then, the matrix $A(x)$ reads

$$A(x) := \begin{pmatrix} A_C C(e) A_C^T & 0 & 0 \\ 0 & L(j_L) & 0 \\ 0 & 0 & 0 \end{pmatrix}, \tag{6}$$

where

$$C(e) := \bar{C}(A_C^T e),\ \bar{C}(u) := \frac{dq(u)}{du} \quad \text{and} \quad L(i) := \frac{d\phi(i)}{di}.$$

The (mostly nonlinear) function $b(x)$ and the vector function r are given by

$$b(x) := \begin{pmatrix} A_R g(A_R^T e) + A_L j_L + A_V j_V \\ -A_L^T e \\ A_V^T e \end{pmatrix} \quad \text{and} \quad r = \begin{pmatrix} -A_I j_s \\ 0 \\ v_s \end{pmatrix}. \tag{7}$$

Before we formulate criteria for the index of DAEs in circuit simulation, we want to prove two basic lemmata.

Lemma 2.1 *If the capacitance and inductance matrices of all capacitances and inductances are p o s i t i v e d e f i n i te then the following relations are satisfied*

$$\ker A(x) = \ker A_C^T \times \{0\} \times \mathbb{R}^{n_V} \quad \textit{and} \quad \operatorname{im} A(x) = \operatorname{im} A_C \times \mathbb{R}^{n_L} \times \{0\},$$

where n_L and n_V denote the number of inductance branches and voltage sources, respectively.

Note, Lemma 2.1 implies that the nullspace $\ker A(x)$ as well as the image space $\operatorname{im} A(x)$ do not depend on x.

Proof: The matrices $C(e)$ and $L(j_L)$ are positive definite since all capacitances and inductances have positive definite capacitance and inductance matrices, respectively. Consider the nullspace of $A(x)$. Obviously,

$$\ker A(x) = \{z = \begin{pmatrix} z_e \\ z_L \\ z_V \end{pmatrix} :\ A_C C(e) A_C^T z_e = 0 \ \wedge\ L(i_L) z_L = 0\}.$$

Lemma 2.2 (next lemma) implies $\ker A_C C(e) A_C^T = \ker A_C^T$. Hence,

$$\ker A(x) = \{z = \begin{pmatrix} z_e \\ z_L \\ z_V \end{pmatrix} :\ A_C^T z_e = 0 \ \wedge\ L(i_L) z_L = 0\}$$

is true. Because of regular $L(j_L)$, we may conclude

$$\ker A(x) = \{z = \left(\begin{smallmatrix} z_e \\ z_L \\ z_V \end{smallmatrix}\right) :\ A_C^T z_e = 0\ \wedge\ z_L = 0\} = \ker A_C^T \times \{0\} \times I\!R^{n_V}.$$

For the image space of $A(x)$ we obtain

$$\text{im } A(x) = \{y = \left(\begin{smallmatrix} y_e \\ y_L \\ 0 \end{smallmatrix}\right) :\ \exists\ \alpha, \beta :\ y_e = A_C C(e) A_C^T \alpha\ \wedge\ y_L = L(j_L)\beta\}. \tag{8}$$

Applying again Lemma 2.2 we have

$$\text{im } A(x) = \{y = \left(\begin{smallmatrix} y_e \\ y_L \\ 0 \end{smallmatrix}\right) :\ \exists\ \bar{\alpha}, \beta :\ y_e = A_C \bar{\alpha}\ \wedge\ y_L = L(i_L)\beta\}.$$

Since $L(i_L)$ is regular,

$$\text{im } A(x) = \{y = \left(\begin{smallmatrix} y_e \\ y_L \\ 0 \end{smallmatrix}\right) :\ \exists\ \bar{\alpha} :\ y_e = A_C \bar{\alpha}\} = \text{im } A_C \times I\!R^{n_L} \times \{0\}.$$

q.e.d.

Lemma 2.2 *If M is a positive definite $m \times m$-matrix and N is a rectangular matrix of dimension $k \times m$, then it holds that*

$$\ker NMN^T = \ker N^T \quad \textit{and} \quad \text{im } NMN^T = \text{im } N.$$

Proof: Consider the nullspace. Obviously, $\ker N^T \subseteq \ker NMN^T$. On the other hand, assume $z \in \ker NMN^T$. Then,

$$z^T NMN^T z = 0, \quad \text{i.e.,} \quad (N^T z)^T M (N^T z) = 0.$$

Since M is positive definite, we may conclude $N^T z = 0$. Therefore,

$$\ker NMN^T = \ker N^T. \tag{9}$$

For the image space we know that $\text{im } NMN^T \subseteq \text{im } N$. Furthermore, relation (9) implies that

$$\text{rank } NMN^T = \text{rank } N^T = \text{rank } N$$

is true, i.e., $\dim(\text{im } NMN^T) = \dim(\text{im } N)$. Hence, $\text{im } NMN^T = \text{im } N^T$ is satisfied.

q.e.d.

For better reading, we call a loop (cf. [2]) containing only capacitances and voltage sources a *Cap-VSRC-loop*. Furthermore, we call a cutset (cf. [2]) containing only inductances and current sources an *Ind-CSRC-cutset*.

Theorem 2.3 *Let the capacitance, inductance and resistance matrices of all capacitances, inductances and resistances, respectively, be positive definite. If the network contains neither Ind-CSRC-cutsets nor controlled Cap-VSRC-loops except for capacitance-only loops, then the MNA leads to an index-1 DAE.*

Note, if the network contains a capacitance-only loop, the Mesh Analysis leads to an index higher than 1 since the current through a capacitance-only loop belongs to the vector of unknowns and represents an index-2 variable. In case of the MNA, the current through a capacitance-only loop does not belong to the vector of unknowns.

Proof: We will show that the DAE (5) is index-1-tractable, i.e., that the matrix $A_1(x) := A(x) + g'(x)Q$ with a constant projector Q onto the nullspace of $A(x)$ is regular. Let Q_C be a constant projector onto $\ker A_C^T$. Regarding Lemma 2.1,

$$Q := \begin{pmatrix} Q_C & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & I \end{pmatrix}$$

represents a constant projector onto $\ker A(x)$. Let

$$G(e) := \bar{G}(A_R^T e), \quad \bar{G}(u) := \frac{dg(u)}{du}.$$

Then the matrix $A_1(x)$ is given by

$$A_1(x) = \begin{pmatrix} A_C C(e) A_C^T + A_R G(e) A_R^T Q_C & 0 & A_V \\ -A_L^T Q_C & L(I_L) & 0 \\ A_V^T Q_C & 0 & 0 \end{pmatrix}. \tag{10}$$

If $z = \left(\begin{smallmatrix} z_e \\ z_L \\ z_V \end{smallmatrix}\right)$ is any vector of the nullspace of $A_1(x)$, then the system

$$\begin{aligned} A_C C(e) A_C^T z_e + A_R G(e) A_R^T Q_C z_e + A_V z_V &= 0, && (11) \\ -A_L^T Q_C z_e + L(i_L) z_L &= 0, && (12) \\ A_V^T Q_C z_e &= 0 && (13) \end{aligned}$$

is true. Multiplying (11) by Q_C^T we obtain

$$Q_C^T A_R G(e) A_R^T Q_C z_e + Q_C^T A_V z_V = 0 \tag{14}$$

since $Q_C^T A_C = (A_C^T Q_C)^T = 0$. Let Q_{VC} be a projector onto $\ker A_V^T Q_C$. Then $Q_{VC}^T Q_C^T A_V = 0$ holds true. Multiplying (14) by Q_{VC}^T yields

$$Q_{VC}^T Q_C^T A_R G(e) A_R^T Q_C z_e = 0. \tag{15}$$

From (13) we know that $z_e \in \ker A_V^T Q_C$, i.e.,

$$z_e = Q_{VC} z_e. \tag{16}$$

Thus, we may write (15) as

$$Q_{VC}^T Q_C^T A_R G(e) A_R^T Q_C Q_{VC} z_e = (Q_{VC}^T Q_C^T A_R) G(e) (Q_{VC}^T Q_C^T A_R)^T z_e = 0.$$

Considering Lemma 2.2 and $G(e)$ to be positive definite, we may conclude

$$A_R^T Q_C Q_{VC} z_e = 0.$$

Applying (16) we obtain

$$A_R^T Q_C z_e = 0. \tag{17}$$

Adding (13), (17) and the trivial relation $A_C^T Q_C z_e = 0$, we obtain

$$(A_V A_R A_C)^T Q_C z_e = 0.$$

Since the network does not contain an Ind-CSRC-cutset, we find a tree (see [2]) of the network containing only capacitive, resistive and VSRC-branches. Hence, the matrix $(A_V A_R A_C)^T$ has full column rank and we may conclude

$$Q_C z_e = 0. \tag{18}$$

Regarding (14) we obtain $Q_C^T A_V z_V = 0$. In [11], we find the fact that the matrix $A_V^T Q_C$ has full row rank if the network does not contain a Cap-VSRC-loop except for capacitance-only loops. Hence, the nullspace of the matrix $Q_C^T A_V$ consists of the zero only. This implies $z_V = 0$. Regarding (11) and (18) again we deduce

$$A_C C(e) A_C^T z_e = 0.$$

Since $C(e)$ is positive definite, Lemma 2.2 implies $A_C^T z_e = 0$, i.e., z_e belongs to the image space of the projector Q_C. Regarding (18) we conclude that $z_e = Q_C z_e = 0$, i.e., the matrix $A_1(x)$ is regular and the network equation system is of index 1.

q.e.d.

Theorem 2.4 *If the network contains Ind-CSRC-cutsets or Cap-VSRC-loops except for capacitance-only loops, then the MNA leads to an index-2 DAE.*

For a complete proof we refer to [11]. Here, we describe the main ideas only.

Choosing the same projectors as in the proof of Theorem 2.3, we construct a non-zero vector belonging to the nullspace of $A_1(x)$.

1. If the network contains an Ind-CSRC-cutset, then this cutset divides the nodes of the network into two groups, e.g. into $\mathcal{N}_1$ and $\mathcal{N}_2$. Let the datum node belong to $\mathcal{N}_2$. Then, $z := (z_e, z_L, z_V)^T$ with

$$z_L := z_V := 0 \quad \text{and} \quad (z_e)_i := \begin{cases} 1 & \text{if} \quad i \in \mathcal{N}_1, \\ 0 & \text{if} \quad i \in \mathcal{N}_2 \end{cases}$$

is an element of $\ker A_1(x)$.

2. If the network contains a Cap-VSRC-loop (excepting capacitance-only loops), then consider all voltage sources of this loop. We define a certain direction for the Cap-VSRC-loop. Then, we divide the voltage sources of the directed loop into two groups $\mathcal{V}_1$ and $\mathcal{V}_2$ in such a way that the k-th voltage source belongs to $\mathcal{V}_1$ if and only if the current of the voltage source has the same direction as the loop direction. This implies that the k-th voltage source belongs to $\mathcal{V}_2$ if and only if the direction of the current of the voltage source and the direction of the loop are distinct. Now, construct $z := (z_e, z_L, z_V)^T$ by

$$(z_V)_k := \begin{cases} 1 & \text{if} \quad k \in \mathcal{V}_1, \\ -1 & \text{if} \quad k \in \mathcal{V}_2, \\ 0 & \text{for all voltage sources outside the loop.} \end{cases}$$

It is not difficult to verify that $Q_C^T A_V z_V = 0$ is true. Since $\text{im } Q_C = \ker A_C^T$ and $C(e)$ is positive definite, the relation

$$\ker Q_C^T = \text{im } A_C = \text{im } A_C C(e) A_C^T = \text{im } A_C C(e) A_C^T (I - Q_C)$$

is satisfied (cf. Lemma 2.2). Hence, we find a $\bar{z}_e$ such that

$$A_V z_V = A_C C(e) A_C^T (I - Q_C) \bar{z}_e.$$

Finally, $z = (z_e, z_L, z_V)^T$ with

$$z_e := -(I - Q_C)\bar{z}_e \quad \text{and} \quad z_L := 0$$

belongs to the nullspace of $A_1(x)$.

Next, we remark that the the intersection

$$\begin{aligned} \ker A \cap S(x) \quad = \quad \{ z : \; & A_C^T z_e = 0, \; A_V^T z_e = 0, \\ & A_R G(e) A_R^T z_e + A_L z_L + A_V z_v \in \text{im } A_C \} \end{aligned}$$

is of constant rank since $G(e)$ is positive definit. It remains to show that

$$N_1(x) \cap S_1(x) = \{0\}$$

is satisfied (see [7]). Regarding (10) the nullspace of $A_1(x)$ is given by

$$N_1(x) = \left\{ z : \begin{array}{rcl} A_C C(e) A_C^T z_e + A_R G(e) A_R^T Q_C z_e + A_V z_V & = & 0, \\ -A_L^T Q_C z_e + L(i_L) z_L & = & 0, \\ A_V^T Q_C z_e & = & 0 \end{array} \right\}$$

Defining $P_C := I - Q_C$ we obtain

$$\begin{array}{rcl} S_1(x) & := & \{z : B_1 z \in \operatorname{im} A_1(x)\} \\ & = & \left\{ z : \exists\ \alpha,\ \gamma : \begin{array}{rcl} A_R G(e) A_R^T P_C z_e + A_L z_L & = & A_R G(e) A_R^T Q_C \alpha \\ & & + A_C C(e) A_C^T \alpha + A_V \gamma, \\ A_V^T P_C z_e & = & A_V^T Q_C \alpha \end{array} \right\} \end{array}$$

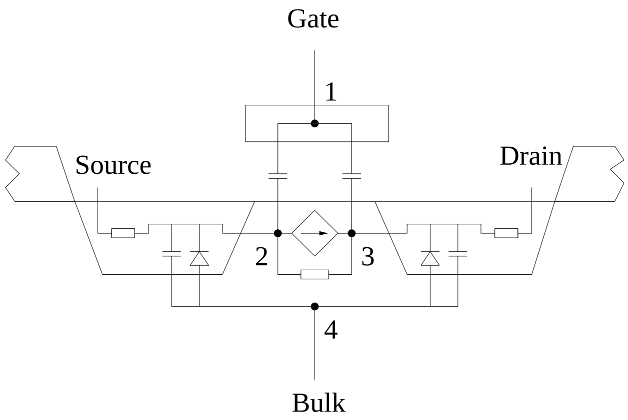
Note, the (reduced) incidence matrix $A = (A_C\ A_L\ A_R\ A_V\ A_I)$ is of constant row rank for lumped circuits (cf. [2]). From an electrotechnical point of view, cutsets of current sources are forbidden. Hence, there is a tree that consists of capacitive brances, inductive brances, resistive branches and branches of voltage sources only. This implies that the matrix $(A_C\ A_L\ A_R\ A_V)$ has full row rank. Using this fact and regarding that $C(e)$, $L(j)$ and $G(e)$ are positive definite it takes some algebraic transformations as in the proof of Theorem 2.3 to show that

$$N_1(x) \cap S_1(x) = \{0\}.$$

Note, a similar result was presented in [9] for networks consisting of linear resistances, inductances and capacitances as well as constant sources, ideal transformers and gyrators. There, it was shown that the branch voltage - branch current equation system has an index not greater than 2. Furthermore, in [6] it was already proved that the T a b l e a u A n a l y s i s for networks containing linear capacitances, resistances and voltage sorces only provides a DAE index 2 if there is a capacitance-VSRC loop in the circuit.

Remarks:

1. Theorem 2.3 and Theorem 2.4 remain valid if the network contains additionally voltage controlled current sources and they are located in the network in the following a way: For each voltage controlled current source, there is a capacitive way between the nodals belonging to the branch whose current is controlled by the source. This fact is important since many networks contain transistor elements, which are often modeled by means of controlled current sources. For an example, we look at a MOSFET model (cf. [3]):



The current from node 2 to node 3 is controlled by the branch voltages v_{GS}, v_{BS} and v_{DS}. Obviously, there is a capacitive way from node 2 to node 3 (via node 1). Hence, Theorem 2.3 and Theorem 2.4 are satisfied for networks containing such MOSFET models.

2. For networks containing any kind of controlled sources, the index can be greater than 2. A simple example of this is a varactor. For a detailed description of higher index cases see [4].

Finally, look briefly at systems obtained by *charge oriented* MNA:

$$A_C\dot{q}_C + A_R r(A_R^T e) + A_L j_L + A_V j_V + A_I j_s = 0, \tag{19}$$
$$\dot{\phi}_L - A_L^T e = 0, \tag{20}$$
$$A_V^T e - v_s = 0, \tag{21}$$
$$q_C = q(A_C^T e), \tag{22}$$
$$\phi_L = \phi(j_L). \tag{23}$$

In comparison with the *charge oriented* MNA, the vector of unknowns additionally consists of the charge of capacitances and of the flux of inductances. Moreover, the original voltage-charge and current-flux equations are added to the system.

Theorem 2.5 *The index of system (19)-(23) coincides with the index of the classical MNA system (2)-(4) for the lower index case (≤ 2).*

Note, $\operatorname{im} A_C = \operatorname{im} A_C q'(A_C^T e) A_C^T$ as well as $\ker A_C^T = \ker A_C q'(A_C^T e) A_C^T$ hold true and ϕ' is regular. Then, following the proof of Theorem 5.6 and 5.7 in [10] we obtain the correctness of Theorem 2.5.

Remark: Theorem 2.5 implies that Theorem 2.3 and Theorem 2.4 are also valid for DAE systems of the form (19)-(23) obtained by charge oriented MNA.

3 Summary

Firstly, we have performed an analysis of networks containing general nonlinear but time-independent capacitances, inductances and resistances as well as independent current sources and independent voltage sources. Then, the MNA for such networks has been shown to lead to a DAE-index 1 if and only if the network contains Ind-CSRC-cutsets or Cap-VSRC-loops (except for capacitance-only loops). Additionally, the DAE-index for these equation systems has been proved to be not greater than 2. Finally, the results remain valid if the networks additionally contain voltage controlled current sources, which are located in the network in such a way that we find a capacitive way between the nodals belonging to the branch the current of which is controlled by the source.

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