Finding Beneficial DAE Structures in Circuit Simulation

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Abstract Circuit simulation is a standard task for the computer–aided design of electronic circuits. The transient analysis is well understood and realized in powerful simulation packages for conventional circuits. But further developments in the production engineering lead to new classes of circuits which may cause difficulties for the numerical integration. The dimension of circuit models can be quite large (10^5 equations). The complexity of the models demands a higher abstraction level. In this paper, we analyze electric circuits with respect to their structural properties. We discuss the relevant subspaces of the resulting differential algebraic equations (DAEs) and present algorithms for calculating the index as well as consistent initial values.

1 Introduction

The modern simulation of electric networks is based on modelling techniques that allow an automatic generation of the model equations. One of the mostly used technique is the Modified Nodal Analysis (MNA). It leads to Differential–Algebraic Equations (DAEs)

$$f(x'(t), x(t), t) = 0. \tag{1}$$

where $f'_{x'}$ is in general singular. For the numerical solution of these special systems arising from circuit simulation, Gear [8] proposed the BDF (Backward Difference Formulae). Their robustness and reliability have made the BDF methods to become a standard in simulation packages up to now. However they failed in certain situations. The study of the theory of DAEs (cf. e.g. [9], [1], [12]) has shown that DAE systems represent not only integration problems but may also involve differentiation problems. DAEs of an index $\geq$ 2 provide solutions including inherent differentiations of the input signals (cf. [10], [15], [16], [6]). These inherent differentiations are not always properly reflected by the BDF methods. Consequently, the variable stepsize BDF usually do not work well for index–3 problems (see e.g. [13]). In the index–2 case, convergence and stability results were obtained for a large class of quasilinear DAEs , e.g. [14], [18], [17].
Naturally, in the analysis of DAEs, various subspaces (and projectors) as e.g. the leading nullspace $f'_{x'}(x', x', t)$ and the tangent spaces to the obvious

and hidden manifolds play an important role. Relevant results – from index characterization up to error propagation – are usually given in terms of those subspaces and projector matrices.
The study of various circuit examples led to the hypothesis that the space of the algebraic components as well as the space of the index–2 components are constant for standard circuit simulation problems. Under these assumptions, convergence and weak instability of the BDF methods is satisfied for index–2 problems [18]. The detailed analysis of circuit systems that we present here enables us to prove the hypothesis to be true for a wide class of circuits (restricted by some conditions for controlled sources, see [4]). Additionally we see that the circuit systems have a special structure that provides fast algorithms for an index check basing on network graphs. This result is really surprising since all other attempts for index tests (using numerical linear algebra) were not always reliable and prohibitively expensive with respect to the circuit simulation itself.
A further nice result of the structural investigations is that in index–2 circuit systems the index–2 components appear only linearly. This can effectively be used for an other practical simulation problem, the calculation of consistent initial values[1]. In section 5 we present a fast and reliable algorithm for computing consistent initial values for circuit systems of index 2.

2 Modeling

The index and the structure of the equations we obtain in electric circuit simulation depend, among other things, on the scheme for setting up the equations (cf. [10], [16]). We will restrict ourselves to two different formulations of the most frequently used modeling technique, the Modified Nodal Analysis.

2.1 Conventional Modified Nodal Analysis

Circuits are usually described in terms of all nodal potentials and currents of current controlled elements. The equation system

$$C(x,t)x' + f(x,t) = 0 \tag{2}$$

contains

- the KCL (Kirchhoff's Current Law) equations and
- the constitutive relations of inductors and voltage sources.

Since the matrix $C(x,t)$ is usually singular, the system (2) represents a quasilinear DAE.

[1] For the definition of consistent initial values see Section 7.

2.2 Charge Oriented Modified Nodal Analysis

In this case, the circuit description bases additionally on the charges of capacitors and fluxes of inductors (y). The resulting equation system

$$\mathcal{A}y' + f(x,t) = 0 \tag{3}$$

$$y = g(x,t) \tag{4}$$

contains again (3)

- the KCL (Kirchhoff's Current Law) equations and
- the constitutive relations of inductors and voltage sources

as well as (4)

- the constitutive relations for capacitors and
- the constitutive relations for inductors.

The matrix $\mathcal{A}$ is usually not quadratically but constant. The equation system (3)–(4) represent so a quasilinear DAE with a constant leading coefficient matrix.

Remark 1. We obtain formulation (2) if we substitute the expression (4) for y into equation (3). The close connection between both formulations allows a transfer of numerous results from one to the other. The charge oriented one is preferred in practice since it guarantees charge and flux conservation automatically (cf. [10]).

2.3 Model Assumptions

We deal with lumped circuits consisting of the following one– and multi–port elements wherein j describes the branch currents and v denotes the branch voltages.

- Passive elements and independent sources
  - Capacitors with the constitutive relation $j = \frac{d}{dt}q_C(v,t)$
  - Inductors with the constitutive relation $v = \frac{d}{dt}\phi_L(j,t)$
  - Resistors with the constitutive relation $j = r(v,t)$
  - Independent current sources described by $j = i(t)$
  - Independent voltage sources described by $v = v(t)$
- Controlled sources
  - Controlled current sources described by $j = i(j,v,t)$
  - Controlled voltage sources described by $v = v(j,v,t)$

  that satisfy certain assumptions (specified in [6]) concerning their location in the network and the kind of controlling variables.

Furthermore, the capacitance matrix $\frac{\partial q_C(v,t)}{\partial v}$, the inductance matrix $\frac{\partial \phi_L(j,t)}{\partial j}$, and the conductance matrix $\frac{\partial r(v,t)}{\partial v}$ are assumed to be positive definite[2].

[2] For capacitors and inductors with affine characteristics the positive definiteness implies that they are strictly locally passive (cf. [7]).

2.4 Detailed Analysis of the Charge Oriented MNA

Splitting the incidence matrix and considering the special properties of the resulting matrices provides a deeper insight into the structure of the equations. If A_C, A_R, A_L, A_V and A_I denote the incidence matrices of the capacitive, resistive, inductive, voltage source and current source branches, respectively, then the charge oriented MNA leads to a system of the form:

$$\begin{aligned} A_C\frac{dq}{dt} + A_R r(A_R^T e,t) + A_L j_L + A_V j_V + A_I i(e,j_L,j_V,t) &= 0,\\ \frac{d\phi}{dt} - A_L^T e &= 0,\\ A_V^T e - v(e,j_L,j_V,t) &= 0,\\ q - q_C(A_C^T e,t) &= 0,\\ \phi - \phi_L(j_L,t) &= 0. \end{aligned}$$

Here, e denotes the nodal voltages, j_L the currents of inductive branches and j_V the currents of voltage source branches. We have summarized the characteristics of independent and controlled current sources by $i(\cdot)$. Correspondingly, the independent and controlled voltage sources are represented by $v(\cdot)$.
Due to Kirchhoff's laws, cutsets of current sources and loops of voltage sources are forbidden. This implies for the element related incidence matrices that

- the matrix (A_C, A_R, A_V, A_L) has full row rank and
- the matrix A_V has full column rank.

3 Index Classification

A long experience in circuit simulation has shown that cutsets of inductors and current sources as well as loops of capacitors and voltage sources may lead to difficulties in the transient analysis. It turns out that these network configurations play (as expected) an essential role in the index classification of networks. Before formulating the result, we introduce some projectors that allow a simple mathematical description of such cutsets and loops. Let

- Q_C be a projector onto $\ker A_C^T$,
- $\bar{Q}_{V-C}$ a projector onto $\ker Q_C^T A_V$, and
- Q_{CRV} a projector onto $\ker(A_C, A_R, A_V)^T$.

Then, the following network characterization is possible.

Lemma 2. *1. If the network does not contain an L–I cutset (a cutset of inductors and/or current sources only (cf. Figure 1)) then the matrix $(A_V, A_R, A_C)^T$ has full column rank and it holds that $Q_{CRV} = 0$.*

2. *If the network does not contain a C–V loop (a loop of capacitors and voltage sources (cf. Figure 1)) then the matrix $Q_C^T A_V$ has full column rank and it holds that $\bar{Q}_{V-C} = 0$.*

Theorem 3. *If the controlled sources satisfy certain topological conditions (specified in [6]) then the DAE system (3)–(4) has an Index ≤ 2. The index is equal 2 if and only if the network contains an L–I cutset or a C–V loop.*

A detailed proof of this theorem is presented in [6].

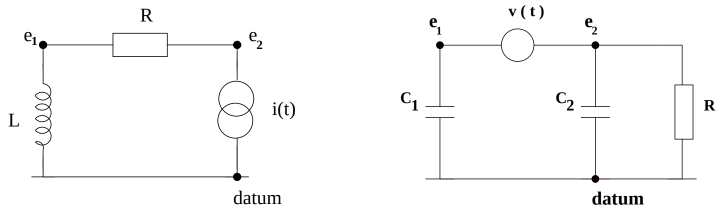

Figure1. Example for an L–I cutset (left) and a C–V loop (right)

Remark 4. 1. Controlled sources in L–I cutsets or C–V loops may lead to arbitrarily high index systems (cf. [11]). Our assumptions for controlled sources (specified in [6]) exclude controlled sources in L–I cutsets or C–V loops.

2. The numerically unstable index–2 components consist of:
   - branch voltages of the inductors and current sources of L–I cutsets and
   - branch currents through voltage sources of C–V loops.

4 Graph–Theoretical Determination of the Hidden Constraints

For the charge–oriented MNA, the hidden constraints result from

$$\frac{d}{dt}\left(\bar{Q}_{V-C}^T A_V^T P_C e - \bar{Q}_{V-C}^T v_t(t)\right) = 0, \tag{5}$$

$$\frac{d}{dt}\left(Q_{CRV}^T A_L j_L + Q_{CRV}^T A_I i_t(t)\right) = 0, \tag{6}$$

and

$$\frac{d}{dt}(q - q_C(A_C^T e, t)) = 0,$$
$$\frac{d}{dt}(\phi - \phi_L(j_L, t)) = 0.$$

Here, the functions i_t and v_t involve only independent current and voltage sources. We are interested in expressions for (5)–(6) without requiring the computation of the corresponding projectors. In [2] it was shown that these equations can be obtained directly from the network by making use of the following two procedures that analyze its graph. In fact, these procedures precisely determine the linearly independent equations that describe the hidden constraints arising from C–V loops and L–I cutsets, respectively.
Let us first focus on the constraints (5) arising from the C–V loops. Recall that

$$A_V^T e - v(\cdot) = 0 \tag{7}$$

are the characteristic equations of the voltage sources. Since $\bar{Q}_{V-C}$ describes the C–V loops, it results that

$$\bar{Q}_{V-C}^T A_V^T e - \bar{Q}_{V-C}^T v_t(t) = 0 \tag{8}$$

corresponds to the sums of the characteristic equations of the voltage sources that form a part of the C–V loops (cf. [2]). More exactly, these equations can be determined by means of the following procedure.

Procedure 1

1. Search a C–V loop in the given network graph. If no C–V loop is found, then end.
2. Write the equation resulting from the sum of the derivatives of the characteristic equations of the voltage sources contained in the C–V loop, taking into account the orientation of the loop and the reference direction of the considered branches.
3. Form a new network graph by deleting the branch of one voltage source that forms a part of the loop, leaving the nodes unchanged.
4. Return to 1, considering the new network graph.

Let us now focus on the constraints (6) arising from L–I cutsets. To get an idea of where they arise from, recall that

$$A_C \frac{dq}{dt} + A_R r(A_R^T e, t) + A_L j_L + A_V j_V + A_I i(\cdot) = 0 \tag{9}$$

are the nodal equations. That means, these equations arise from KCL for the L–I cutsets. Consequently, the equations corresponding to (6) can be determined by means of the following procedure that starts again considering the original graph (cf. [2]).

Procedure 2

1. Search an L–I cutset. If one is found, then select an arbitrary inductor of this cutset. Realize that we can always find such an inductor because cutsets of current sources only are forbidden. If no L–I cutset is found, then end.

2. Write a new equation resulting by differentiation of the cutset equation arising from 1.
3. Delete the chosen inductor from the network contracting its incident nodes.
4. Return to 1, considering the new network graph.

5 Consistent Initialization

Using the graph–theoretical description of the hidden constraints, it is possible to calculate consistent initial values at relatively low costs.
We obtain a consistent initial value starting up from a possibly inconsistent one (x^0) that fulfills the system's equations (for instance, the DC–operating point) in the following way (cf. [3]):

1. Add additional currents that flow through the C–V loops as a consequence of the hidden constraints described by Procedure 1 to the values of the currents through the branches that form a part of C–V loops.
2. Add convenient values to the node potentials to fulfill the additional voltage across the L–I cutsets defined by the hidden constraints described by Procedure 2.

Practical advantage of this approach is that the values that have to be added result by solving a linear system. This system consists of a part of the original DAE together with the equation obtained by Procedure 1 and Procedure 2. The graph–theoretical determination of the relevant equations is very fast with respect to the transient analysis.

6 Computational Aspects and Practical Results

The methods suggested were implemented in the simulation package TITAN[3]. For this purpose, a graph oriented algorithm was developed that provides important features for several aspects:

1. Index determination (cf. Theorem 3).
2. Identification of critical variables: the currents through voltage sources that form a part of C–V loops and the branch voltages of branches that form a part of L–I cutsets.
3. Identification of the circuit elements and nodes which form the critical circuit configurations; this provides valuable information for the user how to regularize higher index configurations in case of problems.
4. Specification of smoothness requirements: Additional smoothness has only to be given for the constitutive relations of the current sources and inductors that form a part of L–I cutsets, and for the characteristic equations of the voltage sources and capacitors that form a part of C–V loops.
5. Description of the linear system that provides the values required for the computation of a consistent initialization.

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6.1 Index Classification

The code was tested for a variety of artificial test circuits and real designs. For some typical MOS circuits without controlled sources, the results are given in Table 1

circuit	transistors	equations	C–V loops	nodes in C–V loops	CPU time
MOS ringoscillator	134	73	3	71	$< 10^{-2}$
16 bit adder	544	283	5	279	0.01
1MBit DRAM	2005	1211	21	1189	0.02
16MBit DRAM	5208	3500	73	3427	0.11
ALU	13005	32639	77	29626	6.76

Table1. Index test for MOS circuits without controlled sources

We observe that all of these circuits are of index 2 due to the existence of C–V loops, and almost all circuit nodes are part of these loops. Furthermore we see that even for large circuits the CPU times (which are measured in sec on a 350 MHz SUN workstation) are very moderate, and the same is true for the circuit examples of Table 2, which contain explicitly given controlled sources.

circuit name	equations	controlled sources	index	CPU time
ringmo	42	8	$= 1$	$< 10^{-2}$
sq3bogner	234	3	$= 2$	$< 10^{-2}$
fischer	2494	10	?	0.04
xsection	13465	958	≥ 2	0.88
clara	35979	2	$= 2$	1.85
teethmi	174881	39	≥ 2	167.01

Table2. Index test for circuits including controlled sources

Note that for the latter class of circuits any index is possible. For some of the circuit examples the index diagnosis is not sharp or even fails. This is due to one of the following reasons:

- The catalogue of conditions specified in [6] is not yet fully implemented.
- The conditions given in [6] are *sufficient* conditions for the index to be ≤ 2; the particular circuit configuration considered here is not (yet) included there.

– In this circuit configuration, the index depends on actual parameter values; in this case structural index diagnosis cannot be successful.

We should mention that controlled sources are implicitely included in any semiconductor device model. Fortunately, the conditions given in [6] state that these controlled sources are not "dangerous" at all, provided that the positive definiteness of the element stamps mentioned before is satisfied. This can be watched during analysis with *local* numerical checks.

6.2 Consistent Initialization

Computational aspects played an important role for the particular development of the methods:

1. Special care was taken to use only those variables which are available in the circuit simulator anyway. The only quantities which had to be extra coded were the time derivatives of the input source functions $i_t(t)$, $v_t(t)$.
2. The algorithm was implemented as an add–on in the simulation flow. In case of index-2 structures the consistent initial values are computed in an extra step from the standard initial values x^0 ("DC–operating point"), which are computed anyway before transient analysis is started.
3. Since the structure of the equations of the resulting linear system is similar to the structure of the original system, part of them can be solved as a structural subset of the original system, taking advantage of the sparse handling. This turns out to be necessary especially in case of C–V loops, which usually cover almost all circuit nodes, see Table 1. Note that this may have an impact on the choice of pivot elements for the linear sparse solver, which are usually selected statically in a preprocessing step in circuit simulation.

As an example, we look at the circuit given in Figure 1 which contains a C–V loop and hence is of index 2. With j_v being the branch current of the voltage source flowing from node 1 to node 2, the MNA equations are:

$$\begin{aligned} j_v + C_1 \cdot e_1' &= 0, \\ -j_v + C_2 \cdot e_2' + 1/R \cdot e_2 &= 0, \\ e_1 - e_2 &= v(t). \end{aligned}$$

The DC–operation point defined by $e_1' = e_2' = 0 \quad \Rightarrow \quad e_1 = v(0), \quad e_2 = 0, \quad j_v = 0$ satisfies these equations, but may violate the hidden constraint

$$e_1' - e_2' = v'(0).$$

For computing a consistent initial solution we assume an additional current $\hat{j}_v$ to flow in the C–V loop, and get

$$\begin{aligned} \hat{j}_v + C_1 \cdot e_1' &= 0, \\ -\hat{j}_v + C_2 \cdot e_2' &= 0, \\ e_1' - e_2' &= v'(0). \end{aligned}$$

Adding the solution to the standard DC–solution, we obtain the following consistent initial values:

$$e_1' = \frac{C_2}{C_1 + C_2} v'(0), \qquad e_2' = -\frac{C_1}{C_1 + C_2} v'(0),$$
$$e_1 = v(0), \qquad e_2 = 0, \qquad j_v = -\frac{C_1 C_2}{C_1 + C_2} v'(0)$$

In practice, the computation of a consistent initialization has been carried out with regard to the following aspects:

1. To start the integration, i.e., in general, the DC operating point is corrected in order to obtain a consistent starting point.
2. To obtain consistent values after discontinuities of the derivatives of the input functions, i.e., at the breakpoints.
3. For a *clean* handling of user given initial conditions by calculating an appropriate x^0 (cf. the approach presented in [3]).

As a practical example shows Figure 2 the waveforms of two index-2 variables of an MOS circuit (word line booster with 124 MOS transistors and 108 equations).
Conventional (dashed) and consistent (solid) waveform differ significantly at the beginning of transient analysis and at the breakpoints, where the slope of input signals changes abruptly. The additional expense for consistent initialization is equivalent to one additional Newton iteration at the beginning and at each breakpoint.

7 Mathematical Background

In this section we summarize new results for specially structured DAEs as described below. The particular properties of the MNA equations guarantee that DAEs arising from circuit simulation have this special structure.

Consider quasilinear DAEs

$$A(x,t)x' + b(x,t) = 0, \tag{10}$$

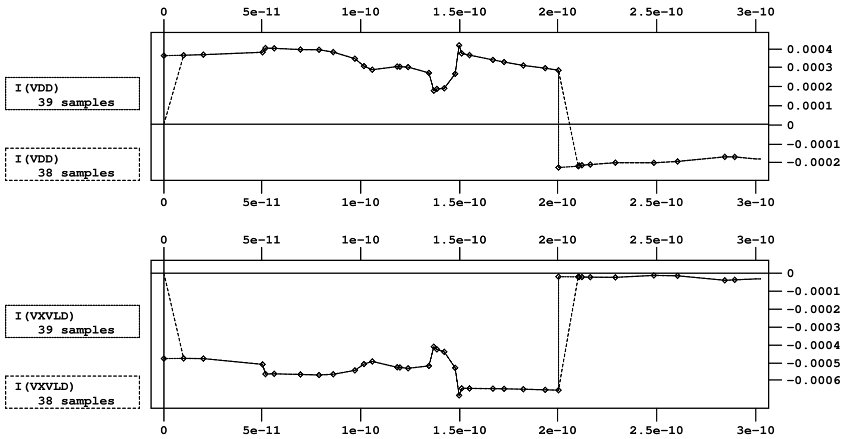

Figure2. Conventional (dashed) and consistent (solid) waveforms for index–2 variables of an MOS circuit

fulfilling that $\ker A(x,t)$ and im $A(x,t)$ are constant. Then, we find constant projectors

$$Q \text{ onto } \ker A(x,t), \quad P := I - Q, \quad \text{and} \quad W_0 \text{ along im } A(x,t).$$

Observe that each solution $x(t)$ of (10) belongs to

$$M_0(t) := \{z : \; W_0 b(z,t) = 0\}, \tag{11}$$

that implies that the choice of initial values for the integration of (10) is restricted. According to ODE theory, we define for DAEs:

Definition 5. A vector $x_0 \in I\!R^n$ is a consistent initial value of (10) if there exists a solution of (10) that fulfills $x(t_0) = x_0$.

In practice, we are also interested in the corresponding values of the derivatives appearing in the DAE. The following definition will characterize these values properly.

Definition 6. A vector (x_0, Py_0) is a consistent initialization of (10), if x_0 is a consistent initial value and (x_0, Py_0) fulfills the equation

$$A(x_0,t_0)Py_0 + b(x_0,t_0) = 0. \tag{12}$$

For the index–1 case, there exists always a solution through a point $x_0 \in M_0(t_0)$ [9], i.e., M_0 describes exactly the set of consistent initial values. Note that the subspace im P may be considered to be a practical substitute of the tangent space to $M_0(t_0)$. For suitably given x^0, condition

$$Px_0 = Px^0 \tag{13}$$

fixes the free integration constants while $r = rank A(x,t) = rank P$ is the dynamical degree of freedom in the index–1 case.
In the higher–index cases, the set of consistent initial values is a proper subset of M_0 that is defined by so called hidden constraints. Let us demonstrate this in detail for index–2 DAEs. Each consistent initial value has to satisfy also the so–called hidden constraint, say equation

$$h(x_0, t_0) = 0. \tag{14}$$

On the other hand, the dynamical freedom decreases in comparison with the index–1 case. By means of an appropriate projector $\Pi = \Pi(x_0, t_0)$ the subspace im Π may be considered to be a practical substitute of the tangent space to

$$M_1(t_0) := \{z \in M_0(t_0), \quad h(z, t_0) = 0\}. \tag{15}$$

This time, for suitably given x^0 the free integration constants are fixed by the condition

$$\Pi(x_0, t_0)x_0 = \Pi(x_0, t_0)x^0. \tag{16}$$

The resulting system (12), (14),(16) to provide a consistent initialization (see e.g. [5]) is somehow difficult to solve. A nice idea ([4]) is now, to use an easily available projector U and to replace the practically very complicated condition (16) by the simple one

$$Ux_0 = Ux^0. \tag{17}$$

The new system (12), (14), (17) is in fact an over–determined extension of (12), (14),(16), supposed $x^0 \in M_0(t_0)$. Then, in the linear case (12), (14), (17) is a consistent linear full rank system and can be solved by least squares.

Let us consider in detail the systems (12), (14),(17) that result if we suppose that the special structure of the MNA equations is given. Suppose that $\ker[A(x,t) + W_0 b'_x(x,t)]$ is constant. Note that this nullspace is identical to $\{0\}$ in case of index–1 DAEs. For index–2 DAEs, this nullspace describes the space of index–2 variables, i.e., the sensitive components with respect to perturbations due to the inherent differentiation problem. We want to assume this space not to be time dependent and even more not to be solution dependent that seems to be natural. For a convenient description we choose constant projectors

$$T \quad \text{onto} \quad \ker[A(x,t) + W_0 b'_x(x,t)] \quad \text{and} \quad U := I - T.$$

Furthermore, we define a projector

$$W_1(x', x, t) \quad \text{along} \quad A(x,t) + ([A(x,t)x']'_x + b'_x(x,t))Q.$$

As a consequence, it results $W_1(x', x, t) = W_1(Ux, t)$ and $W_0 b(x, t) = W_0 b(Ux, t)$. In other words, the projector W_1 as well as the derivative free equations $W_0 b = 0$ are independent of the index–2 components Tx.

Using the above projectors, our investigations have shown [4] that the equations obtained by means of MNA are quasilinear DAEs even of the form

$$A(Ux, t)x' + \tilde{b}(Ux, t) + \mathcal{B}Tx = 0 \tag{18}$$

for a constant matrix $\mathcal{B}$ if the controlled sources of a network satisfy certain conditions specified (cf. [3],[4]), i.e., the index–2 components appear only linear in the DAE system. Obviously, all solutions $x(t)$ of (18) have to satisfy the algebraic relations

$$W_0 \tilde{b}(Ux(t), t) = 0$$

and additionally its derivative[4]

$$\frac{d}{dt} W_0 \tilde{b}(Ux(t), t) = 0. \tag{19}$$

It results for the specific structure that the hidden constraints arise only from the W_1–part of (19), i.e., from

$$W_1(Ux, t)(W_0 \tilde{b})'_x(Ux, t)Px' + W_1(Ux, t)(W_0 \tilde{b})'_t(Ux, t) = 0.$$

Correspondingly, the set of consistent initial values for DAE systems (18) is given by

$$\begin{aligned} M_1(t) := \Big\{ z : \ \exists y \quad & A(Uz, t)y + \tilde{b}(Uz, t) + \mathcal{B}Tz = 0, \\ & W_1(Uz, t)\Big[(W_0 \tilde{b})'_x(Uz, t)y + (W_0 \tilde{b})'_t(Uz, t) \Big] = 0 \Big\}. \end{aligned}$$

As a consequence, consistent initial values can be computed as follows:

Theorem 7. *[4] Suppose that some values (x^0, Py^0) fulfilling*

$$A(Ux^0, t_0)y^0 + \tilde{b}(Ux^0, t_0) + \mathcal{B}Tx^0 = 0$$

are given. We obtain a consistent initialization (x_0, Py_0) starting up from (x^0, Py^0) setting $Ux_0 := Ux^0$, computing the unique solution $(\hat{x}_0, P\hat{y}_0)$ of the linear system

$$\begin{aligned} A(Ux_0, t_0)\hat{y}_0 + \mathcal{B}T\hat{x}_0 &= 0, \\ U\hat{x}_0 &= 0, \\ W_1(Ux_0, t_0)(W_0 \tilde{b})'_x(Ux_0, t_0)P[y^0 + \hat{y}_0] & \\ + W_1(Ux_0, t_0)(W_0 \tilde{b})'_t(Ux_0, t_0) &= 0, \end{aligned}$$

[4] Actually, smoothness is not necessary for complete $W_0 \tilde{b}$. A detailed analysis of smoothness requirements can be found in [4].

and setting

$$x_0 = x^0 + \hat{x}_0,$$
$$Py_0 = Py^0 + P\hat{y}_0.$$

This corresponds to the approach described in Section 5. The realization was achieved making use of the fact that for the equations of the MNA the projectors Q, W_0, T, W_1 can be expressed in terms of the projectors Q_C, $\bar{Q}_{V-C}$, Q_{CRV} introduced in Section 3.

8 Conclusion

Exploitation of the special structure of network equations is beneficial for applying recent results of DAE theory to circuit simulation problems of industrial relevance and complexity. Since the relevant DAE subspaces of the circuit equations can directly be constructed from properly coloured network graphs, it is possible to develop very efficient and reliable methods for

- calculating the DAE index of even very large circuits;
- identifying critical circuit configurations and providing suggestions for their regularization;
- computing consistent initial values;
- implementing a clean handling of user given initial conditions.

A key issue of the approaches presented here is to combine *global topological* criteria – like the existence of C–V loops – with *local numerical* criteria – like the positive definiteness of the device stamps – thus combining the speed of graph oriented methods with the generality and reliability of numerical checks.
The algorithms were successfully implemented into an industrial circuit simulator and have proven to be practical for circuits with more than 10^5 equations. Essential outcomes of this work are, that industry

- has learned how to construct future device and circuit models in order to avoid numerical problems due to too high DAE index as far as possible;
- for the first time, has means to really assess the practical relevance of circuit problems with DAE index > 2.

Actual work is concerned with some desirable extensions of the set of conditions for checking the DAE index, and with industrial efforts to drive the new algorithms into practical use. Furthermore, the methods serve for improvements in the cooperative BMBF projects “Modifizierte ROW–Methoden in der elektrischen Schaltungssimulation” at the TU Karlsruhe, see paper of M. Günther et al. in this issue ($\Rightarrow$ consistent initialization), and “Analyse gemischt analog–digitaler hochoszillierender Schaltungen” at the TU München, see paper of A. Schwarz et al. in this issue ($\Rightarrow$ identification of index-2 configurations, fast construction of projectors onto the relevant subspaces).

Desirable topics for future work in this field are a generalization of the results presented here from topological to structural aspects, the development of practical stability criteria, the structural analysis of circuits including extended semiconductor models and the extension to stochastic DAEs such that noise effects can be efficiently included into transient circuit simulation.

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